EE 330
Homework 1
Fall 2022

Due Monday August 29 at 12:00 noon but accepted without penalty until 11:59 PM on same day.

Problem 1

Assume a simple circuit requires 2,750 MOS transistors on a die and that all transistors are minimally sized. The transistors are fabricated in a 5nm CMOS process with $L_{min} = 5nm$ and $W_{min} = 5nm$ as the minimum gate size. If the actual area (including wiring and isolation) required for making a transistor is 10 times its gate area (i.e., 10X spacing/interconnect overhead), determine the number of die that can be fabricated on a 300mm wafer. Neglect the area required for the bonding pads on the circuit and for sawing the wafer into die.

Problem 2

If the cost of a "12-inch" wafer (which is actually 300mm, but is often called 12-inch for convenience) in 5nm technology is $7250, determine the cost/die for the circuit in Problem 1.

Problem 3

How does the feature size (minimum gate length) in a 5nm process compare to the approximate atomic "diameter" of a silicon atom, to a SiO_2 molecule, and to the diameter of a human hair? How many minimum sized 5nm transistors can be placed on a die that has the same areas as the cross-section of a human hair? (Hint: Google atom/molecule/hair size).

Problem 4

The clock frequency of microprocessors has not increased appreciably for the past 15 years yet performance is improving through the parallelism offered by multiple cores. Why might it be more energy efficient to use multiple cores on a die each operating at a lower clock rate than to have a single core operating at a higher clock frequency?

Problem 5

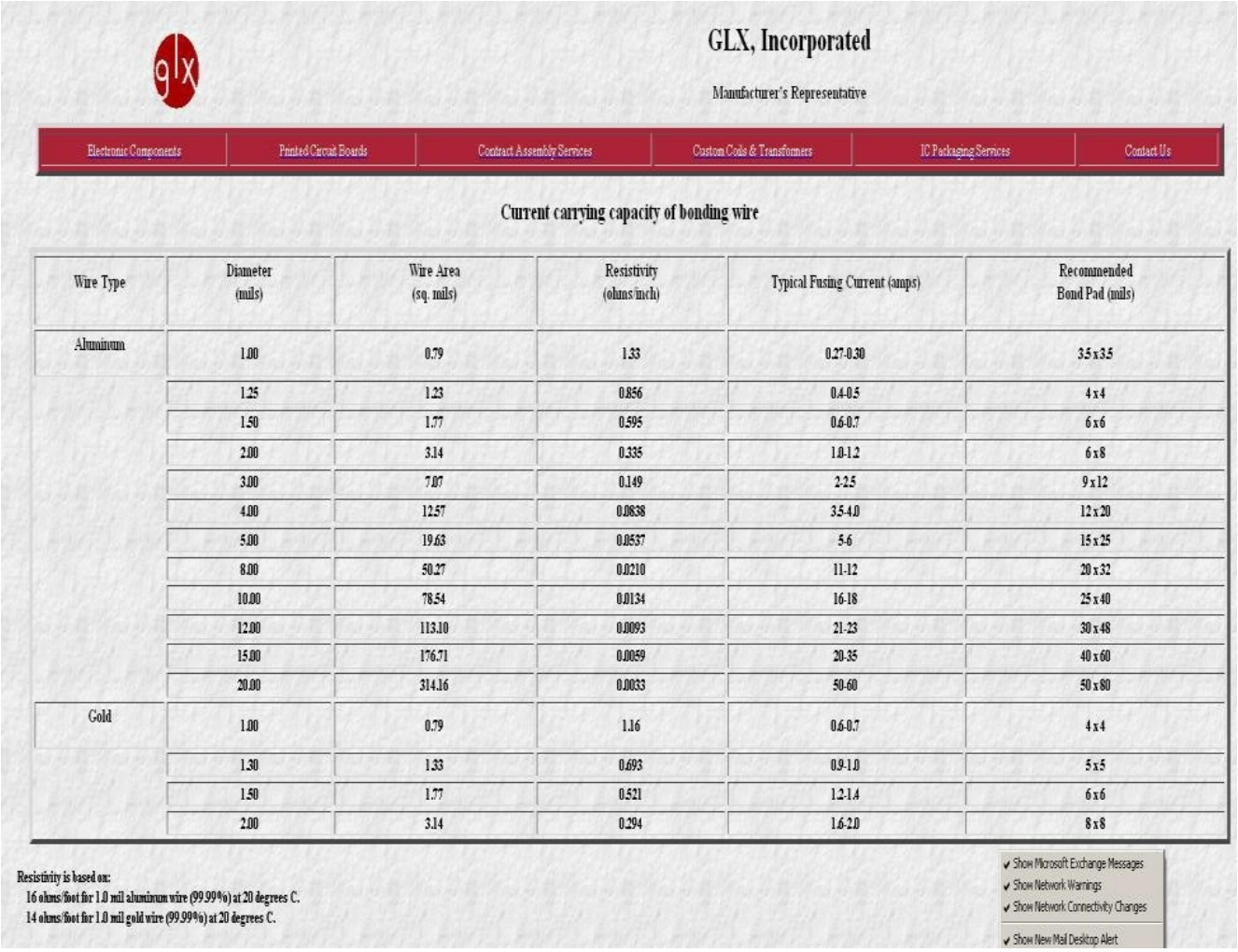
How do the annual sales of semiconductor products of Samsung and Intel compare to the annual sales of Boeing and Nestle? Be quantitative. State the sources for your numbers.

Problem 6

The current flow into a microprocessor can be quite large. There are various methods for connecting a power supply to an integrated circuit, but one way is with gold wires that are termed "bonding wires". Assuming the average supply voltage of the Quad Core Intel i7-9700k is 1.2V and the power dissipation is 95 watts.

a) What is the current draw from the 1.2V supply?
b) What would be the voltage drop in a bonding wire if a single gold wire that is 25.5μ (1 mil) in diameter and ½ inch long is used to bring power into the processor?
c) What would be the power dissipated in this wire?

d) How many parallel gold wires that are 25 µm in diameter would be needed to guarantee that the current in these interconnects is at most 10% of the fusing current (from image)?



GLX, Incorporated

Manufacturer's Representative

Electronic Components | Printed Circuit Boards | Contract Assembly Services | Custom Coils & Transformers | IC Packaging Services | Contact Us

Current carrying capacity of bonding wire

Wire Type	Diameter (mils)	Wire Area (sq. mils)	Resistivity (ohms/inch)	Typical Fusing Current (amps)	Recommended Bond Pad (mils)
Aluminum	1.00	0.79	1.33	0.27-0.30	3.5 x 3.5
	1.25	1.23	0.856	0.4-0.5	4 x 4
	1.50	1.77	0.595	0.6-0.7	6 x 6
	2.00	3.14	0.335	1.0-1.2	6 x 8
	3.00	7.07	0.149	2-2.5	9 x 12
	4.00	12.57	0.0838	3.5-4.0	12 x 20
	5.00	19.63	0.0537	5-6	15 x 25
	8.00	50.27	0.0210	11-12	20 x 32
	10.00	78.54	0.0134	16-18	25 x 40
	12.00	113.10	0.0093	21-23	30 x 48
	15.00	176.71	0.0059	20-35	40 x 60
	20.00	314.16	0.0033	50-60	50 x 80
Gold	1.00	0.79	1.16	0.6-0.7	4 x 4
	1.30	1.33	0.693	0.9-1.0	5 x 5
	1.50	1.77	0.521	1.2-1.4	6 x 6
	2.00	3.14	0.294	1.6-2.0	8 x 8

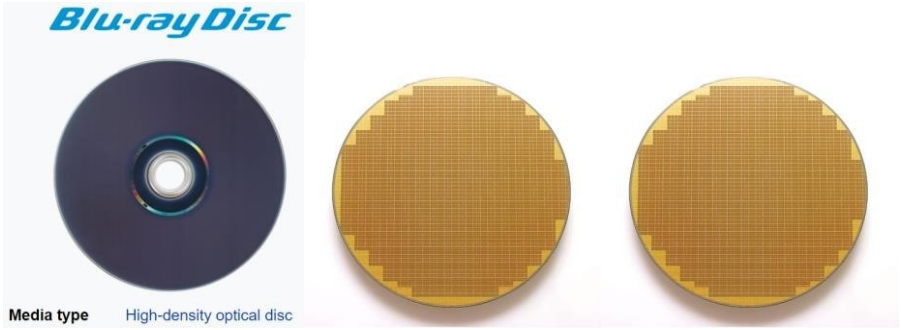
Resistivity is based on:
16 ohms/foot for 1.0 mil aluminum wire (99.99%) at 20 degrees C.
14 ohms/foot for 1.0 mil gold wire (99.99%) at 20 degrees C.

Figure 1: Some properties of gold and aluminum wires

Problem 7-8

Data is stored in many different ways but today the most popular strategies for storage that can be rapidly retrieved are CDs, DVDs, Blu Ray DVDs, hard disks, static memory (SRAM), dynamic memory (DRAM), and Flash Memory. The first three store data physically on metal/plastic media and retrieve it optically. Hard disks store data magnetically. SRAMs and DRAMs store data electronically in semiconductor materials. Flash memory devices store data electronically in floating gate transistors. Using a table, make a comparison of the storage density (bits per cm^2) and the commercial cost of storage per bit in these 7 different media. In making this comparison, try to use state of the art parts or components and, when appropriate, state which part you are using and the approximate cost for the component or device.

Based upon this comparison, what is the lowest cost method for storing data and what is the ratio in the cost/bit between the most expensive and the least expensive data storage approaches in this comparison?



Problem 9

What percent of the smart phones today use Android? IOS? What about Windows OS? Give the sources of your data.

Problem 10

How many smart phones were sold worldwide in 2021? What percent uses Android, iOS, and Windows OS? How many smart phones were used worldwide in 2021? Based on the "sold" and "in use" ratio, comment on the useful "life" of a smart phone. Give the sources of your data.

Problem 11

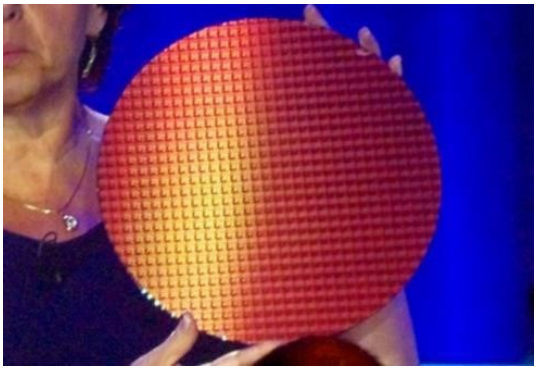
A major engineering effort is required to support the mobile-phone industry. This includes engineers that work all the way from the infrastructure level down to the process development level. Using the number of smart phone users in the world and worldwide annual smart-phone sales obtained in the previous problem, obtain a very approximate estimate of the level of the engineering workforce that is needed to support the smart phone industry. In making this assessment, make the following basic simplifying assumptions. Assume the average smartphone selling price is $500 (this is not the "plan" price) and the average salary of engineers is $85,000 (of course some get paid much more and some much less in different parts of the world). If 10% of the total mobile-phone sales revenue is invested in the salary of engineers responsible for development of the mobile-phone infrastructure, how many full-time engineers are needed worldwide to support the growing mobile-phone industry?

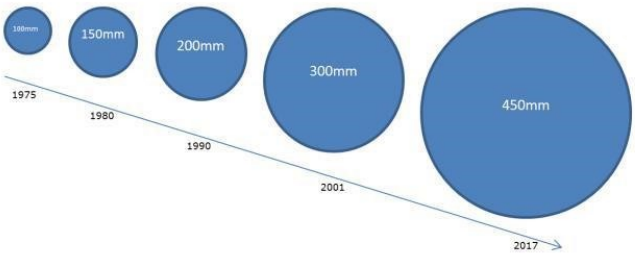
Problem 12

A picture of a woman holding a $450mm$ wafer of Intel Skylake chips is shown below on the left. Standard wafer sizes in the industry are shown below on the right.

a) Determine the approximate number of Skylake chips on this wafer

b) If the yield is 90% and the manufacturing costs for the wafer are $7500, what is the cost of manufacturing a Skylake chip?





Problem 13

How many electrical conductors are in a USB 2 cable and a USB 3 cable? What is the use of each of these conductors? How is USB 2 backwards compatibility achieved with a USB 3 cable?